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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,374	03/12/2004	Minoru Suzuki	016907-1612	5644

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FOLEY AND LARDNER LLP
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WASHINGTON, DC 20007

EXAMINER

RADKIEWICZ, JARED

ART UNIT	PAPER NUMBER
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2609

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/798,374

Applicant(s)

SUZUKI, MINORU

Examiner

Jared W. Radkiewicz

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 3/12/2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: Image Processing Apparatus for Efficient Storage of Variable Block Length Data. Appropriate correction is required.

Claim Objections

2. Claim 1 is objected to because of the following informalities: the term "bit" is used inappropriately in claim 1. The term is apparently being used to refer to "a small piece or quantity of anything", however in the art the term has a special meaning of a binary digit, or a "single, basic unit of information, used in connection with computers and information theory". This misuse is evident in the phrase "length of the bit", as binary digits do not have length. For the examination of this application the examiner will make a judgment of which "bits" are binary digits and which are a collection of binary digits, the latter being designated by an asterisk (*) herein. Appropriate correction is required.

3. Claim 3 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

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Claim 3 describes removing the added bits from a uniform block to become a variable length block, just like in claim 1 paragraph 5: "variable-length codes obtained by erasing the added bits from the variable-length codes of the all blocks". Also, claim 1 paragraph 3 describes the bit-length storage of claim 3. Claim 3 does uniquely ascribe this action to the "block-data-length conversion" section, yet this term is vague enough to be interpreted as all block length conversions occurring in the apparatus, and does not sufficiently further limit claim 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goris et al. (US 6,157,743) in combination with Mishra (US 6,298,404 B1).

Regarding claim 1, Goris teaches an image processing apparatus comprising:

a variable-length compression section that performs variable-length compression on image data of each block included in one page ("JPEG, run-length encoding, Huffman encoding", Goris Column 2 Lines 15-16);

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an adjusting section which adjusts each block to a constant data length by adding a bit* to or truncating part of a variable-length code of each block obtained by compression by the variable-length compression section ("Then, the segment size for data structure 400 may be set equal to the largest of compressed blocks 0-n (i.e., the block having the worst case compression ratio). In this manner, the amount of system memory wasted by unused portions such as portions 404, 406 and 408 will be minimized", Goris Column 7 Lines 44-49);

a bit*-length storage which stores a data length of the bit* added by the adjusting section to the variable-length code of each block ("Preferably, header 502 will contain a block length field 504, the purpose of which is to indicate the length of the compressed block contained in that segment", Goris Column 7 Lines 62-64);

a variable-length-code storage which stores variable-length codes obtained by erasing the added bits from the variable-length codes of the all blocks ("a first technique for storing variable-length blocks of compressed texture data in a memory system. Data structure 200 includes a number of compressed texture data blocks 0-n. Compressed blocks 0-n do not have a common block length. Nevertheless, they are stored contiguously in system memory 104", Goris Column 6 Lines 50-55); and

a block-data-length conversion section which adds respective bits* of different data lengths to variable-length codes of blocks read from the variable-length-code storage, converting data lengths of the blocks into a shorter constant data length than the constant data length, if the determination section determines

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that the respective bits are added to the all blocks, the different data lengths being obtained by subtracting a shortest data length from a data length of each block stored in the bit*-length storage ("Then, the segment size for data structure 400 may be set equal to the largest of compressed blocks 0-n (i.e., the block having the worst case compression ratio). In this manner, the amount of system memory wasted by unused portions such as portions 404, 406 and 408 will be minimized", Goris Column 7 Lines 44-49).

Goris does not teach a determination section which determines whether the adjusting section has added respective bits to all blocks included in the one page.

Mishra teaches the concept of operating on small blocks of a full-page image and a determination section that determines when all blocks have been processed ("step 338 determines if all blocks in the buffer (the buffer containing the M main-scan lines) have been rotated and written to the appropriate place in memory", Mishra Column 15 Lines 62-64; although Mishra uses the block processing method with respect to a rotation algorithm, the principle of sequentially processing individual blocks of an image and determining when the entire image has been processed is being taught).

It would have been obvious at the time of invention to one of ordinary skill in the art to use the compression storage scheme of Goris in the apparatus of Mishra because Mishra's apparatus processes images in "blocks of 32 bytes ... results[ing] in a very efficient transfer of images" (Mishra Column 5 Lines 22-23). Furthermore, Mishra's apparatus has capabilities to apply "various image

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manipulation functions" (Mishra Column 12 Line 62) to images. By applying Goris' "efficient technique for storing and retrieving" (Goris Column 3 Line 6) image data to Mishra's apparatus the system has become even more efficient which would allow Mishra to maintain high page per minute processing capabilities.

6. Regarding claim 2, Goris and Mishra teach the image processing apparatus according to claim 1, wherein if the determination section determines that the respective bits are not added to the all blocks, the block-data-length conversion section adds respective bits of data lengths, stored in the bit-length storage, to the variable-length codes of the blocks read from the variable-length-code storage, converting the data length of each block into the constant data length ("Data structure 500 is the same in all respects to data structure 400, except that a header 502 has been added to the beginning of each segment", Goris Column 7 Lines 59-62; "Then, the segment size for data structure 400 may be set equal to the largest of compressed blocks 0-n (i.e., the block having the worst case compression ratio). In this manner, the amount of system memory wasted by unused portions such as portions 404, 406 and 408 will be minimized", Goris Column 7 Lines 44-49).

7. Regarding claim 3, Goris and Mishra teach the image processing apparatus according to claim 1, wherein the block-data-length conversion section

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erases the added bit from each variable-length code of the constant data length, based on the data length of each bit stored in the bit-length storage and stores the variable-length code in the variable-length-code storage ("a first technique for storing variable-length blocks of compressed texture data in a memory system. Data structure 200 includes a number of compressed texture data blocks 0-n. Compressed blocks 0-n do not have a common block length. Nevertheless, they are stored contiguously in system memory 104", Goris Column 6 Lines 50-63).

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goris et al. (US 6,157,743) and Mishra (US 6,298,404 B1) in further view of Mishra (US 6,298,404 B1).

Regarding claim 4, Goris and Mishra teach the image processing apparatus according to claim 1, further comprising:

an erasure section which erases, before printing, the bit added to the variable-length code of each block supplied from the page memory, based on a determination result of the determination section and the data length of each bit stored in the bit-length storage (Figure 8A describes the compressed image retrieval mechanism including determining data length stored and removing null data).

Goris and Mishra do not teach the image processing apparatus according to claim 1, further comprising:

a page memory which temporarily stores the variable-length code of each block, the variable-length code having the constant data length; and

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Mishra teaches a page memory which temporarily stores the variable-length code of each block, the variable-length code having the constant data length ("Mass Storage" 20 Mishra Figure 1);

It would have been obvious at the time of invention to one of ordinary skill in the art to provide the apparatus of Goris and Mishra with the page memory of Mishra as the storage unit of Goris.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goris et al. (US 6,157,743) and Mishra (US 6,298,404 B1) in further view of Silverbrook (US 5,329,616).

Regarding claim 5, Goris and Mishra teach claim 1.

Goris and Mishra do not teach the image processing apparatus according to claim 1, wherein the variable-length compression section performs joint photographic experts group processing.

Silverbrook teaches JPEG as a variable length compression scheme. ("JPEG ADCT compressed data because that data is of variable length", Silverbrook Column 6 Lines 37-39).

It would have been obvious at the time of invention to one of ordinary skill in the art to use JPEG compression as the variable length compression in Goris and Mishra because it is a standard well known to those in the art.

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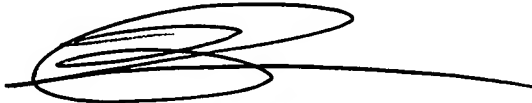
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared W. Radkiewicz whose telephone number is (571) 270-1577. The examiner can normally be reached on 8:00 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian P. Werner can be reached on (571) 272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JWR

A handwritten signature in black ink, consisting of a stylized 'B' followed by a horizontal line.

BRIAN WERNER
SUPERVISORY PATENT EXAMINER